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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/888,271	06/21/2001	Robert Y. Greenberg	7293-15	8636

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EXAMINER	
TRAN, TRANG U	

ART UNIT	PAPER NUMBER
2614	

DATE MAILED: 02/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/888,271	GREENBERG, ROBERT Y.
	Examiner	Art Unit
	Trang U. Tran	2614

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-17* is/are allowed.

6)☒ Claim(s) *18-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 13, 2004 has been entered.

Response to Arguments

2. Applicant's arguments with respect to claims 18-42 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 18-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cappels, Sr. (US Patent No. 5,731,843) in view of Ichiraku (US Patent No. 6,097,379).

In considering claim 18, Cappels, Sr. discloses all the claimed subject matter, note 1) the claimed an edge detector adapted to generate an edge pulse corresponding to a transition of an analog image signal responsive to a pixel

clock is met by the differentiator 52 and the threshold detector 44 which is function together to detect voltage transitions between pixel instructions, also called pixels edges (Fig. 3, col. 4, lines 42-59), 2) the claimed a phase adjust circuit to generate the pixel clock responsive to the phase adjust signal is met by the phase adjuster 50 which produces an adjusted pixel sampling clock 64 that matches the phase of the video signal 52 (Figs. 3 and 4, col. 5, line 15 to col. 6, line 31), and 3) the claimed a phase detector circuit to generate the phase adjust signal responsive to the edge pulse signal is met by the phase comparator 46 and the microprocessor 48 (Fig. 3, col. 4, line 60 to col. 5, line 27).

However, Cappels, Sr. explicitly does not disclose the claimed a phase adjusting circuit to generate the pixel clock by selecting one of a plurality of phases of a phase locked loop clock.

Ichiraku teaches that as is shown in Fig. 3, the phase adjusting circuit 2 of the present invention is provided with: a sampling clock generating circuit for detection 21, into which a standard clock (PCLK) which is synchronized with a horizontal synchronizing signal is inputted, and which divides this standard clock (PCLK) into a number m (a positive integer) of standard clocks, and which applies, with respect to these standard clocks, a delay amount proportional to the amount of the cycle thereof divided by m, and which generates and outputs, in stages, a number m of sampling clocks for detection (DPCLK [0,1,2,...,m]) having different phases... and a selecting circuit 22, which accepts as an input the sampling clocks for detection 21, controls these by means of the control signal, selects the appropriate sampling clock for detection from among these,

and outputs this as the sampling clock (SCLK) to the pixel data sampling circuit (Fig. 3, col. 8, line 43 to col. 9, line 40).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the delay clocks (DPCLK [0,1,2,...,m]) having different phases and the selection as taught by Ichiraku into Cappels, Sr.'s system in order to accurately produce the sampling clock signal having an appropriate phase for sampling pixel data of the video signal.

In considering claim 19, the claimed wherein the edge detector generates the edge pulse signal responsive to the transition of the analog data signal greater than a predetermined threshold is met by the differentiator 95 and the threshold detector 100 which is function together to produce the pulse signal if the applied voltage pulse exceeding a predetermined threshold voltage (Figs. 3 and 5, col. 2, lines 5-28 and col. 6, lines 32-57 of Cappels, Sr.).

In considering claim 20, the claimed wherein the edge detector generates the edge pulse responsive to a rising, falling, or both rising and falling edges of the analog image signal is met by the voltage transition location 20 which occurs between a change in voltage levels and between discrete pixel intensities 19 on video signal 12 (Fig. 1, col. 3, lines 6-43 of Cappels, Sr.).

In considering claim 21, the claimed wherein the edge detector comprises a calibration circuit adapted to calibrate the analog image signal with the pixel clock is met by the automatically adjusting the pixel sampling clock frequency and phase to match the frequency and phase of the pixel clock used to generate an incoming video signal (col. 1, lines 60-64 of Cappels, Sr.).

In considering claim 22, the claimed wherein the phase adjust circuit is adapted to adjust the phase of the pixel clock by delaying the reference signal is met by the delay circuit 12 (Fig. 1, col. 6, line 66 to col. 7, line 52 of Ichiraku).

In considering claim 23, Ichiraku discloses the claimed wherein the phase adjust circuit comprises: a clock delay circuit adapted to generate a plurality of delayed clock signals by delaying the phase locked loop clock is met by the delay clocks (DPCLK [0,1,2,...,m]) having different phases (Fig. 3, col. 8, line 43 to col. 9, line 40), and the claimed a multiplexer adapted to select one of the plurality of delayed clock signals as the pixel clock responsive to a phase adjust signal is met by the selecting circuit 22 which selects the appropriate sampling clock for detection and outputs this as the sampling clock (SCLK) to the pixel data sampling circuit (Fig. 3, col. 8, line 43 to col. 9, line 40).

In considering claim 24, the claimed wherein the clock delay circuit comprises an n-stage delay locked loop, each stage generating a corresponding delayed clock phase, each delayed clock phase being 360/n degrees out of phase is met by the delay clocks (DPCLK [0,1,2,...,m]) having different phases (Fig. 3, col. 8, line 43 to col. 9, line 40 of Ichiraku).

In considering claim 25, Cappels, Sr. discloses all the claimed subject matter, note 1) the claimed wherein the phase adjust circuit comprises a clock delayed circuit to generate the plurality of clock phases by delaying the phase locked loop clock signal is met by the phase adjuster (phase shift of Fig. 4) 50 which produces an adjusted pixel sampling clock 64 that matches the phase of the video signal 52 (Figs. 3 and 4, col. 5, line 15 to col. 6, line 31), 2) the claimed

wherein the phase detector comprises: a phase hit enable signal adapted to generate a plurality of phase hit enable signals corresponding to each of the plurality of clock phases, the phase hit enable signal being asserted responsive to the edge pulse signal is met by the hit detection process (Fig. 5, col. 4, line 60 to col. 5, line 27 and col. 6, line 58 to col. 7, line 37), and 3) the claimed a count corresponding to each of the plurality of clock phases, the count indicative of a number of assertions of a corresponding phase hit enable signal for over a predetermined time is met by the microprocessor 48 stores in memory 49 a number representing the total hits for that specific phase (col. 5, lines 3-27).

In considering claim 26, the claimed wherein the phase detector circuit comprises: an enable signal to enable the phase detector circuit is met by the Q-output pulse 108 from the one-shot pulse generator 81 is true, data line 112 is set high, indicating that a "hit", a sampling edge in close temporal proximity to a video transition, has taken place (Fig. 5, col. 6, line 58 to col. 7, line 37), and the claimed a clear signal to clear each count is met by the NOT-Q output 118 of one-shot pulse generator 81, the latch 82 is reset to await for the next edge detection (Fig. 5, col. 6, line 58 to col. 7, line 37 of Cappels, Sr.).

In considering claim 27, the combination of Cappels, Sr. and Ichiraku discloses all the limitations of the instant invention as discussed in claims 18 and 25 above, except for providing the claimed wherein the predetermined time is a number of image scan lines. The capability of using the predetermined time is a number of image scan lines is old and well known in the art. Therefore, the Official Notice is taken. It would have been obvious to one of ordinary skill in the

art at the time of the invention to incorporate the old and well known of using the predetermined time is a number of image scan lines into the combination of Cappels, Sr. and Ichiraku's system since it merely amounts to selecting an alternative equivalent edge detector.

In considering claim 28, the claimed comprising: a phase detector circuit generates phase adjust signals by analyzing the count is met by the microprocessor 48 which calculates a hit percentage for each varies phase and the hit percentage is the number of hits for a given number of video edges at a given phase to obtain which phase is the maximum number of hits, then the microprocessor 48 can determine the phase of the sampling clock with respect to the horizontal synchronization pulse that will provide the optimum sampling of the incoming video signal 52 (Fig. 4, col. 5, line 15 to col. 6, line 31 of Cappels, Sr.).

In considering claim 29, the claimed comprising a phase locked loop circuit adapted to derive the clock signal from the reference signal responsive to a frequency adjust signal is met by the pixel sampling clock 55 which is a conventional phase-locked loop using a programmable divider and coupled to the horizontal sync pulse (Fig. 3, col. 4, lines 35-42 of Cappels, Sr.).

Claim 30 is rejected for the same reason as discussed in claim 16.

The method claim 31, Cappels, Sr. discloses all the claimed subject matter, note 1) the claimed detecting a transitions of an analog signal responsive to a pixel clock signal is met by the differentiator 52 and the threshold detector 44 which is function together to detect voltage transitions between pixel instructions, also called pixels edges (Fig. 3, col. 4, lines 42-59), 2) the claimed asserting a

clock phase hit responsive to the determining is met by the hit detection process (Fig. 5, col. 4, line 60 to col. 5, line 27 and col. 6, line 58 to col. 7, line 37), 3) the claimed counting a number of clock phase hits for each of the clock phases is met by the hit detection process (Fig. 5, col. 4, line 60 to col. 5, line 27 and col. 6, line 58 to col. 7, line 37), and 4) the claimed generating a phase and frequency adjust signal as the result of the counting is met by the microprocessor 48 stores in memory 49 a number representing the total hits for that specific phase (Fig. 5, col. 4, line 60 to col. 6, line 31).

However, Cappels, Sr. explicitly do not the claimed generating a plurality of clock phases by delaying a phase lock loop clock signal by a plurality of delays, and determining which of the plurality of clock phases corresponds to the transition by substantially simultaneously comparing the transition to the plurality of clock phases.

Ichiraku teaches that as is shown in Fig. 3, the phase adjusting circuit 2 of the present invention is provided with: a sampling clock generating circuit for detection 21, into which a standard clock (PCLK) which is synchronized with a horizontal synchronizing signal is inputted, and which divides this standard clock (PCLK) into a number m (a positive integer) of standard clocks, and which applies, with respect to these standard clocks, a delay amount proportional to the amount of the cycle thereof divided by m, and which generates and outputs, in stages, a number m of sampling clocks for detection (DPCLK [0,1,2,...,m]) having different phases... and a selecting circuit 22, which accepts as an input the sampling clocks for detection 21, controls these by means of the control

signal, selects the appropriate sampling clock for detection from among these, and outputs this as the sampling clock (SCLK) to the pixel data sampling circuit (Fig. 3, col. 8, line 43 to col. 9, line 40).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the delay clocks (DPCLK [0,1,2,...,m]) having different phases and the selection as taught by Ichiraku into Cappels, Sr.'s system in order to accurately produce the sampling clock signal having an appropriate phase for sampling pixel data of the video signal.

Claim 32 is rejected for the same reason as discussed in claim 29.

Claim 33 is rejected for the same reason as discussed in claim 23.

Claim 34 is rejected for the same reason as discussed in claim 19.

Claim 35 is rejected for the same reason as discussed in claim 20.

In considering claim 36, the claimed wherein detecting a transition includes generating an edge pulse responsive to the transition and wherein asserting a clock phase hit includes comparing the edge pulse with each of the clock phase is met by the hit detection process (Fig. 5, col. 4, line 60 to col. 5, line 27 and col. 6, line 58 to col. 7, line 37 of Cappels, Sr.).

In considering claim 37, the claimed wherein asserting the clock phase hit includes generating a plurality of clock phase hit signals corresponding to the plurality of clock phases and asserting only the clock phase hit signal closest to the transition is met by the hit detection process (Fig. 5, col. 4, line 60 to col. 5, line 27 and col. 6, line 58 to col. 7, line 37 of Cappels, Sr.).

Claim 38 is rejected for the same reason as discussed in claim 25.

Claim 39 is rejected for the same reason as discussed in claim 27.

Claim 40 is rejected for the same reason as discussed in claim 26.

In considering claim 41, the claimed wherein counting includes generating a count for each of the clock phases and wherein counting comprises: examining the count; and adjusting the frequency of the pixel clock if the count exceeds a predetermined number is met by is met by the microprocessor 48 can determine the phase of the sampling clock with respect to the horizontal synchronization pulse that will provide the optimum sampling of the incoming video signal 52 by determining which phase obtains a maximum number of hits and the microprocessor 48 using line 67 to vary the pixel clock frequencies via the pixel clock 55 until a single, distinct, optimum setting is obtained (Fig. 4, col. 5, line 15 to col. 6, line 31 of Cappels, Sr.).

In considering claim 42, the claimed wherein adjusting the frequency of the pixel clock comprises: changing the frequency of the clock signal; clearing the count; enabling the count; repeating the counting, examining, and adjusting if the count exceeds a predetermined number is met by is met by the microprocessor 48 can determine the phase of the sampling clock with respect to the horizontal synchronization pulse that will provide the optimum sampling of the incoming video signal 52 by determining which phase obtains a maximum number of hits and the microprocessor 48 using line 67 to vary the pixel clock frequencies via the pixel clock 55 until a single, distinct, optimum setting is obtained (Fig. 4, col. 5, line 15 to col. 6, line 31 of Cappels, Sr.).

Allowable Subject Matter

5. Claims 1-17 allowed.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trang U. Tran whose telephone number is (703) 305-0090. The examiner can normally be reached on 8:00 AM - 5:30 PM, Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John W. Miller can be reached on (703) 305-4795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TRANG TRAN
PATENT EXAMINER

TT
February 19, 2005